

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:
 - 5 a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and
 - 10 a main reset signal generator for generating a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.
 2. A semiconductor integrated circuit according to claim 1, wherein said main reset signal generator comprises:
 - 15 a plurality of pulse generators for respectively generating a pulse in synchronization with a transition edge for each of said sub power-on reset signals; and
 - 20 a composite circuit for synthesizing the pulses to generate said main power-on reset signal.
 3. A semiconductor integrated circuit comprising:
 - 25 a sub reset signal generator for generating a sub power-on reset signal;
 - 30 a reset terminal for receiving an external power-on reset signal; and
 - 35 a main reset signal generator for generating a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.
 4. A semiconductor integrated circuit according to claim 3, wherein said main reset signal generator comprises:
 - 30 a plurality of pulse generators for respectively generating a pulse in synchronization with a transition edge for each of said sub power-on reset signal and said external power-on reset signal; and
 - 35 a composite circuit for synthesizing said pulses to generate said main power-on reset signal.
 5. A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

5 a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

10 6. A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

15 a plurality of pulse generators for respectively generating a pulse in synchronization with a transition edge for each of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

7. A method of initializing a semiconductor integrated circuit comprising the steps of:

20 generating a plurality of power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other; and

initializing an internal circuit according to at least one from any of said power-on reset signals.